**Factory Acceptance Test Report**

**DRAFT TEMPLATE – *Not to be used***

[Project name]

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**[Student Name – college no]**

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**[Course Name]**

**[Date]**

Version 1.0

VERSION HISTORY

|  |  |  |  |
| --- | --- | --- | --- |
| **Version No** | **Implemented**  **By** | **Document Change Notice\*** | **Summary of change** |
| 0.1 | ZB |  | First draft |
| 0.2 | ZB |  | Internal Review |
| 1.0 | ZB | DCN 1234 | First approved release |
|  |  |  |  |

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# INTRODUCTION

# IDENTIFICATION

This document is the Final Acceptance Test (FAT) Report for Heritage College third year EIT program students final project titled <Project Name>. It is identified as EIT-<year>-<projectName>-FAT, version 1.0

# purpose

Purpose of the document is to report the latest Factory Acceptance Test (FAT) results and recommendation for the fabrication release of the project’s Printed Circuit Board (PCB).

# document overview

The document introduces first the project, then describes the test activities planned to achieve this verification effort, followed by a description of the test cases, and results. Outstanding issues are captured and recommendation for PCB production is provided last.

# GLOSSARY

The following terms and acronyms are used throughout the report

|  |  |
| --- | --- |
| PCB | Printed Circuit Board |
| FAT | Factory Acceptance Testing |
| TBD | To Be Determined |
| EIT | Electronics and Information Technology |
|  |  |

# referenceS

The following documents are referred throughout this report:

|  |  |  |  |
| --- | --- | --- | --- |
| ID | Title | Date | version |
| R1 | Project Charter | XX-SEP-2022 | 1.0 |
| R2 | Project Preliminary Presentation |  |  |
| R3 | Development and Test Process standard |  |  |
| R4 | Methodology guideline |  |  |
| R5 | College / EIT Laboratory Safety standards |  |  |
|  |  |  |  |

# TEST PLAN

# Test items (functions)

The plan is to test all electronic components on or attached to main PCB.

# RISK ISSUES

The following table list all the part that will be tested.

|  |  |  |
| --- | --- | --- |
| RI-01 | Original Requirements |  |
|  | Power Safety |  |
|  | Connections |  |
|  | Reverse polarity |  |
|  | Logic level conversion |  |
|  | … |  |

# Features not to be tested

The following features are not tested

|  |  |
| --- | --- |
| ID |  |
| U-01 |  |
| U-02 |  |
| … |  |

# approach (strategy)

Our overall test strategy for this plan is as follows:

Tools: We will use the following tools to …

Metrics: We will collect the following data during the tests:

Configuration Management (CM) will handle as follows:

Only/Many versions of the configuration will be tested.

Only the electronics components will be tested.

# ITEM PASS/FAIL CRITERIA

The criteria for this completion of test plan is that:

1. all test cases have been completed
2. test cases with minor defects are tracked using issues

# Test DELIVERABLES

# Test cases

# Test results

# issue list

# environmental needs

voltmeter

power supply

pc workstation

Arduino IDE version 1.X

# staffing and training needs

# Responsabilities

*Who will do what?*

# schedule

# planning risks and contingencies

# Approvals

Who will:

1. approve the process as complete?
2. Allow the project to proceed to the next level?

|  |  |  |
| --- | --- | --- |
| ID | Features | Risk Level  (L/M/H) |

## 

| **Step** | **Instructions** | **Expected Result** | **Actual Result** | **Pass/Fail** |
| --- | --- | --- | --- | --- |
| 1 | Locate the application’s .exe file or the equivalent shortcut | N/A | N/A | N/A |
| 2 | Double-click on the .exe file to open the application | The application opens onto the main window. |  | N/A |

# 3.0 TEST CASES

# 4.0 test RESULTS

This section will be completed after completion of the final FAT.

# 5.0 RECOMMENDATIONS

This section will be completed after completion of the final FAT.

# 6.0 TEST RESULT APPROVALs

# TBD